Application No.: 10/777,902 Docket No. 10017912-3 (1509-239A)

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously presented) A circuit comprising a first terminal for connection to a voltage source having first and second levels and a transition between the levels, a driver including first and second opposite conductivity type transistors, each including a control electrode and a path arranged to be switched on and off in response to a voltage applied to the control electrode being on opposite sides of a threshold level, the first and second transistor paths being connected in series across opposite power supply terminals, an output terminal between the paths, circuitry connected between the first terminal and the control electrodes for causing the first and second transistor paths to be respectively (a) in on and off states while the voltage source has the first level and (b) in off and on states while the voltage source has the second level, said circuitry including at least one voltage responsive switchable capacitor connected (a) to be responsive to voltage at the first terminal and (b) to the driver for preventing the paths of the first and second transistors from being on simultaneously during transitions between the on and off states of the first and second transistor paths, the at least one switchable capacitor being arranged to have an initial finite capacitance value during an initial part of the transition between the levels and to be switched from the initial finite capacitance value to a substantially open circuit in response to the voltage across the at least one switchable capacitor changing during the transition between the levels from one side of a threshold voltage to a second side of the threshold voltage, the threshold voltage being between the first and second levels.

2. (Canceled)

3. (Previously presented) The circuit of claim 1 wherein the at least one switchable capacitor is connected between one of the control electrodes and a DC power supply terminal of the circuit.

4. (Previously presented) The circuit of claim 3 wherein the circuitry further includes a resistive element connected to supply current to the at least one switchable capacitor in response to the voltage at the first terminal.

5. (Canceled)

6. (Previously presented) The circuit of claim 28, wherein the circuitry further includes a resistive element connected to supply current to the at least one switchable capacitor in response to the voltage at the first terminal, wherein said PFET of said driver, said NFET of said driver and said at least one switchable capacitor are included on an integrated circuit chip, and said resistive element comprises a resistor.

7. (Canceled)

8. (Previously presented) The circuit of claim 1 wherein the at least one switchable capacitor includes first and second voltage controlled switchable capacitors

respectively connected to delay coupling of the transitions to the control electrodes of the first and second transistors.

9. (Previously presented) The circuit of claim 8 wherein said first and second capacitors are respectively connected between the control electrodes of the transistors and the opposite power supply terminals are respectively first and second power supply terminals of the circuit and are such that (a) the first capacitor is arranged to have a finite capacitance value on a first side of a first voltage threshold and a substantially open circuit on a second side of the first threshold, and (b) the second capacitor is arranged to have a finite capacitance value on a second side of a second voltage threshold and a substantially open circuit on a first side of the second threshold, the first and second thresholds differing from each other and being between the first and second levels.

10. (Canceled)

11. (Previously presented) The circuit of claim 9 wherein the circuitry further includes first and second resistive elements respectively connected to supply current to the first and second capacitors in response to the voltage at the first terminal.

12. (Previously Presented) The circuit of claim 11 wherein the first and second transistors are respectively a PFET and an NFET and the first and second capacitors are respectively an NFET and a PFET.

13. (Previously Presented) The circuit of claim 12 wherein the first and second transistors, the first and second resistive elements, and the first and second capacitors are included on an integrated circuit chip, the first and second resistive elements including first and second resistors on the chip.

14. (Previously presented) The circuit of claim 8 wherein the circuitry further includes first and second inverters each having (a) an input terminal for enabling the first and second inverters to be simultaneously responsive to the voltage at the first terminal and (b) an output terminal, the output terminal of the first inverter being connected to supply current via a first DC path to the first capacitor and the control electrode of the first transistor to the exclusion of the second capacitor and the control electrode of the second transistor, the output terminal of the second inverter being connected to supply current via a second DC path to the second capacitor and the control electrode of the second transistor to the exclusion of the first capacitor and the control electrode of the first transistor.

15. (Previously presented) The circuit of claim 14 wherein the first and second transistors are field effect transistors, the first and second inverters comprise field effect transistors, and the first and second capacitors comprise field effect transistors.

16. (Previously presented) The circuit of claim 15 wherein all of the field effect transistors are included on an integrated circuit chip including first and second resistors

respectively connected with the first and second transistors and the first and second inverters.

17. (Original) The circuit of claim 16 wherein the first and second resistors are respectively included in the first and second inverters.

18. (Previously presented) The circuit of claim 8 wherein

the first and second transistors are respectively a PFET and an NFET, the circuitry further includes first and second inverters, each of the first and second inverters having (a) an input terminal for enabling the first and second inverters to be simultaneously responsive to the voltage at the first terminal and (b) an output terminal, the output terminal of the first inverter being connected to supply current via a first DC path to the first capacitor and the control electrode of the first transistor, the output terminal of the second inverter being connected to supply current via a second DC path to the second capacitor and the control electrode of the second transistor, each of the inverters including a PFET and an NFET, the PFET and NFET of each inverter having a source drain path and a gate electrode having a connection to the first terminal so that the gate electrodes of the PFETs and NFETs of the inverters are driven in parallel by the voltage at the input terminal, the output terminal of each of the inverters being between the source drain paths of the PFET and NFET thereof,

the first and second capacitors comprise field effect transistors,

all of the field effect transistors are included on an integrated circuit chip including first and second resistors respectively connected with the first and second field effect transistors and the first and second inverters, and

the first and second resistors are respectively included in the first and second inverters.

19. (Original) The circuit of claim 18 wherein the first resistor is connected between the source drain path of the NFET of the first inverter and the output terminal of the first inverter, the second resistor being connected between the source drain path of the PFET of the second inverter and the output terminal of the second inverter.

20. (Original) The circuit of claim 19 wherein the first and second capacitors respectively include an NFET and a PFET.

21. (Original) The circuit of claim 20 wherein the NFET and PFET included in the first and second capacitors respectively have different first and second thresholds between the first and second levels, the NFET included in the first capacitor having a finite capacitance value for voltages below the first threshold and being a substantially open circuit for voltages greater than the first threshold, the PFET included in the second capacitor having a finite capacitance value for voltages greater than the second threshold and being a substantially open circuit for voltages less than the second threshold, the first threshold being greater than the second threshold.

22. (Previously presented) A method of operating a driver including first and second opposite conductivity type transistors, each including a control electrode and a path between a pair of further electrodes controlled in response to a voltage applied to the control electrode, the paths of the first and second transistors being connected in series across opposite first and second power supply terminals, an output terminal between the series connected paths, a first switchable capacitor connected between the control electrode of the first transistor and the first power supply terminal and a second switchable capacitor connected between the control electrode of the second transistor and the second power supply terminal, the method comprising: during a first interval: causing the paths of the first and second transistors to be respectively, on and off, while the second capacitor is charged and the first capacitor is switched off by applying (a) a first voltage having a first value to the control electrode of the first transistor, (b) the first voltage value across the second capacitor, and (c) a second voltage having the first value to the control electrode of the second transistor; during a second interval: causing the paths of the first and second transistors to be off and on, respectively, while the second capacitor is switched off and the first capacitor is charged by applying (a) a second value of the first voltage to the control electrode of the first transistor, (b) the first voltage value across the first capacitor, and (c) the second value of the second voltage to the control electrode of the second transistor; during an initial portion of a first transitional period between the first and second intervals: turning off the path of the first transistor while maintaining the path of the second transistor off by changing the first voltage from the first value toward the second value while the first capacitor remains switched off and the second capacitor is charged; during a second portion of the first transitional period turning on the path of the

second transistor while maintaining the path of the first transistor off by changing the charge on the second capacitor so that there is a change in the value of the second voltage from the first value toward the second value; during an initial portion of a second transitional period between the second and first intervals: turning off the path of the second transistor while maintaining the path of the first transistor off by changing the second voltage from the second value toward the first value while the second capacitor remains switched off and the first capacitor is charged; and during a second portion of the second transitional period turning on the path of the first transistor while maintaining the path of the second transistor off by changing the charge on the first capacitor so that there is a change in the value of the first voltage from the second value toward the first value.

23. (Original) The method of claim 22 further comprising the steps of: switching off the first capacitor during the second portion of the first transitional period prior to the value of the first voltage, as applied to the control electrode of the first transistor, reaching the first value; and switching off the second capacitor during the second portion of the second transitional period prior to the value of the second voltage, as applied to the control electrode of the first transistor, reaching the second value.

24. (Previously presented) The method of claim 23 wherein the first and second capacitors are charged and switched off in response to the first and second voltages having values on opposite sides of first and second thresholds respectively associated with the first and second capacitors.

25. (Previously presented) The circuit of claim 9, wherein the first and second transistors are respectively a PFET and an NFET and the first and second capacitors are respectively an NFET and a PFET, the first transistor having a source drain path connection to a positive power supply terminal, the second transistor having a source drain path connection to a negative power supply terminal, the positive and negative power supply terminals respectively being the first and second power supply terminals, the first capacitor having a first electrode connected to the gate electrode of the first transistor and a second electrode connected to the negative power supply terminal, the second capacitor having a first electrode connected to the gate electrode of the second transistor and a second electrode connected to the positive power supply terminal.

26. (Currently amended) A driver having an input terminal adapted to be responsive to a bi-level signal, the driver including first and second opposite conductivity type transistors, each including a control electrode and a path between a pair of further electrodes controlled in response to a voltage applied to the control electrode, the paths of the first and second transistors being connected in series across opposite first and second power supply terminals, an output terminal between the series connected paths, a first switchable capacitor connected between the control electrode of the first transistor and the second power supply terminal, a second switchable capacitor connected between the control electrode of the second transistor and the first power supply terminal, the first and second transistors having first and second thresholds between the voltages at the first and second power supply terminals so that the paths of

the first and second transistors are arranged to be on and off in response to the voltages applied to the control electrodes being on opposite sides of the first and second thresholds thereof, the first and second capacitors respectively having third and fourth thresholds between the voltages at the first and second power supply terminals for causing the capacitors to have finite values and be switched off in response to the voltages across the capacitors being on opposite sides of the third and fourth thresholds;

the control electrodes and the capacitors being connected to each other and to the input terminal, the connections of the capacitors to the control electrode and to the input terminal and the first, second, third and fourth thresholds being such that in response to:

(I) a first transition between the levels of the bi-level signal that extends in a first direction, (a) the second capacitor is switched off and the voltage across the second capacitor and at the control electrode of the second transistor suddenly changes toward the voltage at the second power supply terminal in response to the voltage across the second capacitor crossing the fourth threshold, (b) the first transistor is turned off and remains turned off until after a second transition between the levels of the bi-level signal that extends in a second direction, (c) the first capacitor has finite values until after the second transition, (d) the second transistor (i) is initially off while the first transistor is off, and (ii) then turns on in response to the voltage across the second capacitor and at the control electrode of the second transistor gradually changing in a direction extending from the voltage at the second power supply terminal toward the

voltage at the first power supply terminal and crossing the second threshold, and (iii) stays on until the second transition occurs, and~~, and~~

(II) the second transition, (a) the first capacitor is switched off and the voltage across the first capacitor and at the control electrode of the first transistor suddenly changes toward the voltage at the first power supply terminal in response to the voltage across the first capacitor crossing the third threshold, (b) the second transistor is turned off and remains turned off until after the first transition, (c) the second capacitor has finite values until after the first transition between the levels of the bi-level signal that extends in a second direction, (d) the first transistor (i) is initially off while the first transistor is off, and (ii) then turns on in response to the voltage across the first capacitor and at the control electrode of the first transistor gradually changing in a direction extending from the voltage at the second power supply terminal toward the voltage at the first power supply terminal and crossing the first threshold, and (iii) stays on until the first transition occurs.

27. (Previously presented) The driver of claim 26, wherein the first and second transistors are respectively a PFET and an NFET, the first and second capacitors are respectively N and P doped FET devices, and the voltages adapted to be connected to the first and second power supply terminals are respectively positive and negative relative to each other, the N doped FET capacitor device being connected so it does not affect current flowing between the input terminal and the gate electrode of the NFET second transistor and the P doped FET capacitor device being connected so it

does not affect current flowing between the input terminal and the gate electrode of the PFET first transistor.

28. (Previously presented) The circuit of claim 1 wherein said first and second transistors are respectively a PFET and an NFET, the opposite power supply terminals being respectively first and second power supply terminals, the first power supply terminal being adapted to be connected to a voltage having a higher value than the voltage adapted to be connected to the second power supply terminal, said at least one switchable capacitor comprising a PFET having (a) a gate electrode connected to the gate electrode of the NFET second transistor, (b) a source electrode, and (c) a drain electrode, the source and drain electrodes of the PFET switchable capacitor being connected to the first power supply terminal, the PFET capacitor being connected so it does not affect current flowing between the input terminal and the gate of the PFET first transistor.

29. (Previously presented) The circuit of claim 1 wherein said first and second transistors are respectively a PFET and an NFET, the opposite power supply terminals being respectively first and second power supply terminals, the first power supply terminal being adapted to be connected to a voltage having a higher value than the voltage adapt to be connected to the second power supply terminal, said at least one switchable capacitor comprising an NFET having (a) a gate electrode connected to the gate electrode of the PFET first transistor, (b) a source electrode, and (c) a drain electrode, the source and drain electrodes of the NFET capacitor being connected to

the second power supply terminal, the NFET capacitor being connected so it does not affect current flowing between the input terminal and the gate of the NFET second transistor.

30. (Previously presented) The circuit of claim 29 further comprising another switchable capacitor comprising a PFET having (a) a gate electrode connected to the gate electrode of the NFET second transistor, (b) a source electrode, and (c) a drain electrode, the source and drain electrodes of the PFET capacitor being connected to the first power supply terminal, the PFET capacitor being connected so it does not affect current flowing between the input terminal and the gate of the PFET first transistor.